REMARKS

This is in full and timely response to the above-identified Office Action. The above listing of the claims replaces all prior versions, and listings, of claims in the application. Reexamination and reconsideration in light of the proposed amendments and the following remarks are respectfully requested.

Rejection under 35 USC § 102

The rejection of claims 9 10 and 12-14 as being anticipated by Harper (USP 6,675,316) is respectfully traversed.

The claimed subject matter, as stated at page 2, lines 14 to 21, of the originally filed specification, relates to solving the problem of providing, in a distributed multiple processing (DMP) system, high-speed access to an external shared memory. A DMP system comprises (see page 1, lines 30 to 32 of the originally filed specification) a number of separate machines or hosts connected through a local area network or other network. An alternative configuration to a DMP system is that of a symmetric processing system (SMP). As described at page 1, lines 13 to 20, (of the originally filed specification) in an SMP system several processors are provided on the same machine - i.e. each processor shares the same memory devices and the same I/O devices.

Independent claim 9 is directed towards a distributed multiple processing system, as opposed to a symmetric processing system. Harper, on the other hand, clearly relates to a symmetric processing system. At first glance, Figure 1 of Harper appears to show one or more hosts (101a) connected to a network (104) giving access to memory nodes (103) and I/O nodes 102. However, a closer inspection shows that the network 104 is in fact that of an internal bus of a computer system. For example, column 5, lines 16 to 25, states that "[T]he CPU/cache, memory and I/O nodes are connected by the interconnect network...". Column 5, lines 10 to 15, states that "[T]he I/O nodes reside on the interconnect network and allow the CPU/cache and memory nodes to pass data to the environment ***external*** to the computer system, via devices such as network disks, serial communication, and parallel communication". Thus, the memory nodes 103 are clearly internal memory nodes and are **NOT** external memory.

Column 9, lines 49 to 60, and Figure 6, disclose that "[T]he CPUs 611 are interconnected via a system bus 612...". Figure 6 confirms the above position inasmuch as a communications adapter 634 is provided for access to external network.

The interpretation that Harper relates to a DMP is therefore deemed to be incorrect and is therefore traversed.

It is therefore submitted that Harper does not disclose a distributed multiprocessing system comprising at least two hosts connected to a network and does not disclose a fault tolerant external memory. It is also submitted that Harper neither discloses that each host further comprises an access device unit connected to the external memory unit, nor discloses that each access device provides each host with a transparent access to the external memory unit.

Thus, the rejection of claim 9 is submitted to be untenable for at least the reasons advanced above, and is therefore traversed.

Regarding the remaining claims, the rejection of claims 10-14 are submitted to be untenable on the basis that Harper does not disclose an external memory.

In connation with claims 13 and 14, there is no disclosure in Harper of the coherency control chipset being arranged as a memory-mapped connection arrangement - the rejection of this subject matter apparently having been derived entirely from an interpretation of Figure 2 which is submitted to not convey the information alleged.

Rejections under 35 USC § 103

The rejection of claims 15-17 under 35 USC § 103(a) as being unpatentable over Harper in view of Duso et al. (USP 6,625,750), is respectfully traversed.

This rejection is submitted to be untenable for at least the reason that the anticipation rejection of claim 1 has been shown to be untenable. Further, the introduction of the teachings of Duso et al. is not seen as providing a hypothetical person of ordinary skill with the necessary guidance to establish a *prima facie* case of obviousness.

Conclusion

Claims 9-10 and 12-17 are submitted as being patentable over the cited references for at least the reasons advanced above. Favorable reconsideration and allowance of these claims along with claim 11 is respectfully requested.

Respectfully submitted,

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By _____

HEWLETT-PACKARD COMPANY
Customer No.: 022879

William T. Ellis
Registration No. 26,874

Keith J. Townsend
Registration No. 40,358